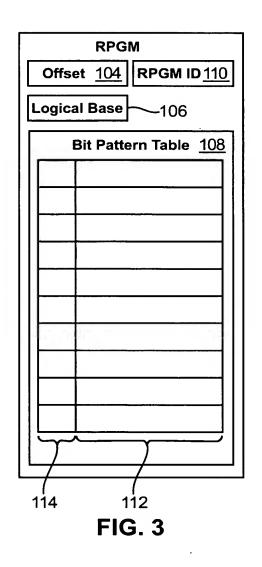
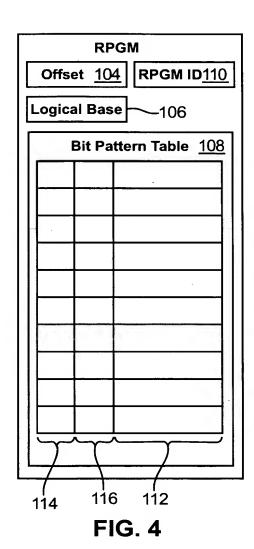


FIG. 2







#### **Pattern Return Process**

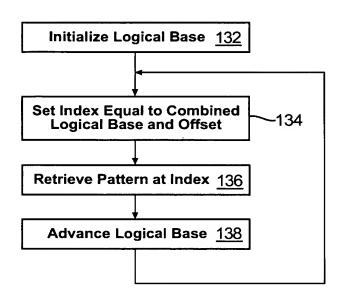


FIG. 5

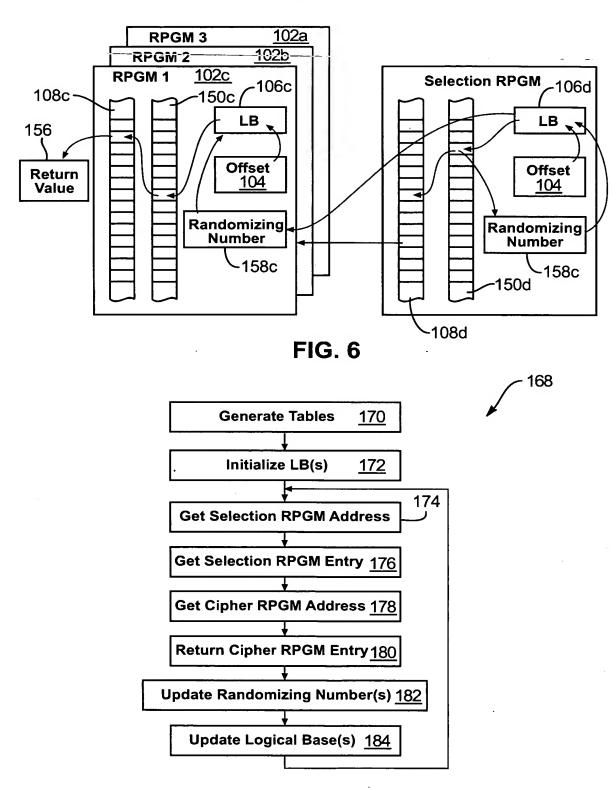


FIG. 7

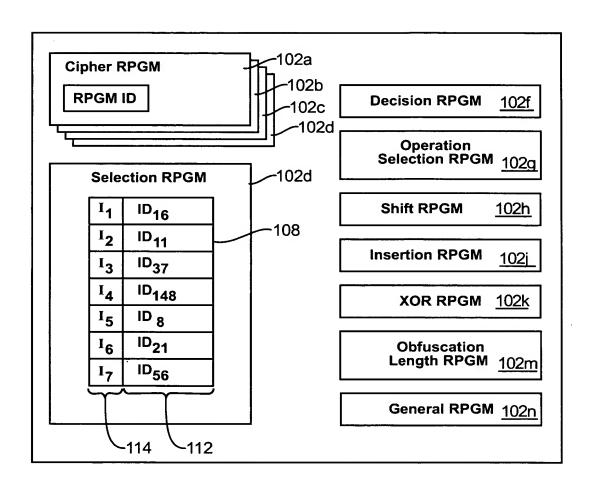


FIG. 8

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	Aggregate	Heterogeno	ous Bit F	<u>Pattern</u>	_204 (	_200
<u>202a</u> \$	202a Segments				Segments	<u>202b</u>
	Slack Bits		Segm	ents	"	
		Segment	s			
Slack Bits	Segme	ents Segments				
	Slack Bits		;	Segme	nts	
Slack Bits		Segn	nents		50.000	

FIG. 9

204~	L	ogical	Base Ta	ble	206	
Logical Base 106c	Slack Bits	L	ogical B	ase	Sla	ack Bits 204
Logical Base 106a	Base Slac 106a Bits				Logical Base 106d	
Slack Bits	Logical I	Base Slack Bits Logical Base			Base	
Logical Base Slack Bits		Logical Base			Slack Bits	
Logical Base			Slack	Bits		

FIG. 10

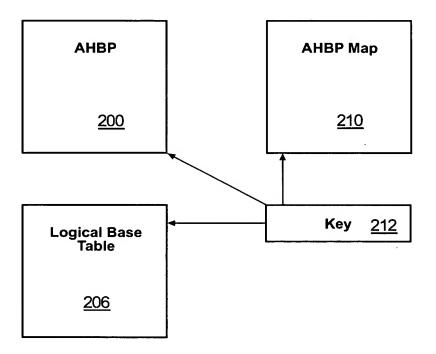


FIG. 11

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RPGM Record	<u>218</u>
RPGM ID 2	220
Starting AHBP Address	<u>222</u>
Segment Count	<u>224</u>
Max Segment Length	<u>226</u>
Number of Entries	<u>228</u>
Bits Per Entry	<u>230</u>
Logical Base Information Bits Per Entry	232
RPGM LBT Address	<u>234</u>
Segment ID(s)	<u>236</u>
AHBP ID	<u>238</u>

FIG. 12

 Segment Record	<u>246</u>
AHBP ID	<u>248</u>
Segment Number	<u>250</u>
Segment Address	<u>252</u>
Segment Length	<u>254</u>
First Entry Address	<u>256</u>
Entry Count	<u>258</u>
Entry Number of First Entr	у <u>260</u>
Address of Last Entry	<u> 262</u>
Last Entry Length	<u>264</u>
Filler Entry Length	<u>266</u>

FIG. 13

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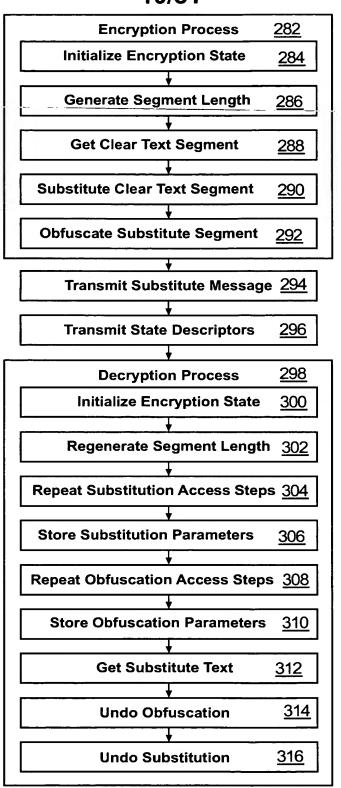


FIG. 14

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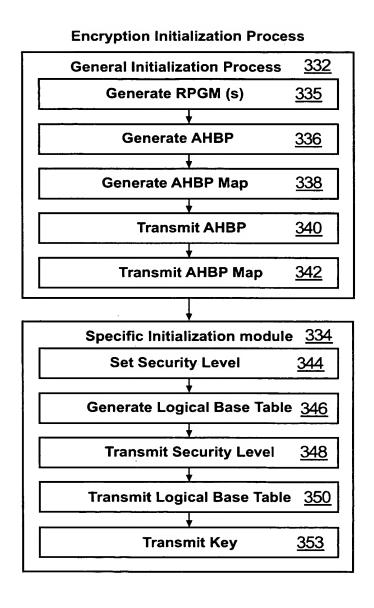


FIG. 15

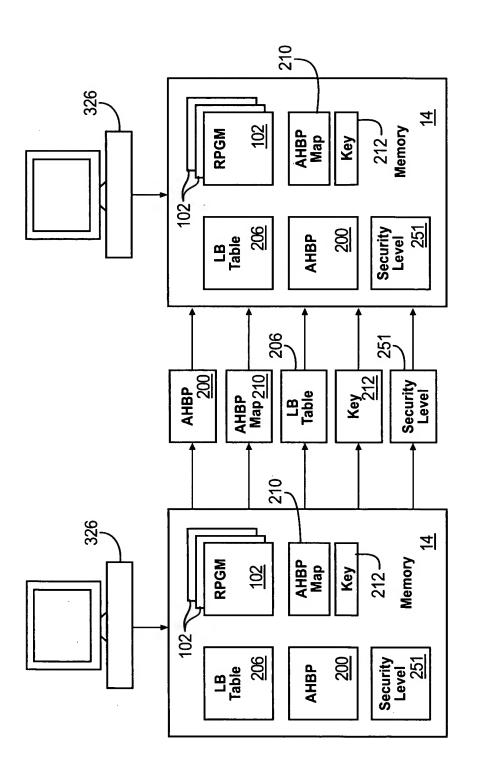
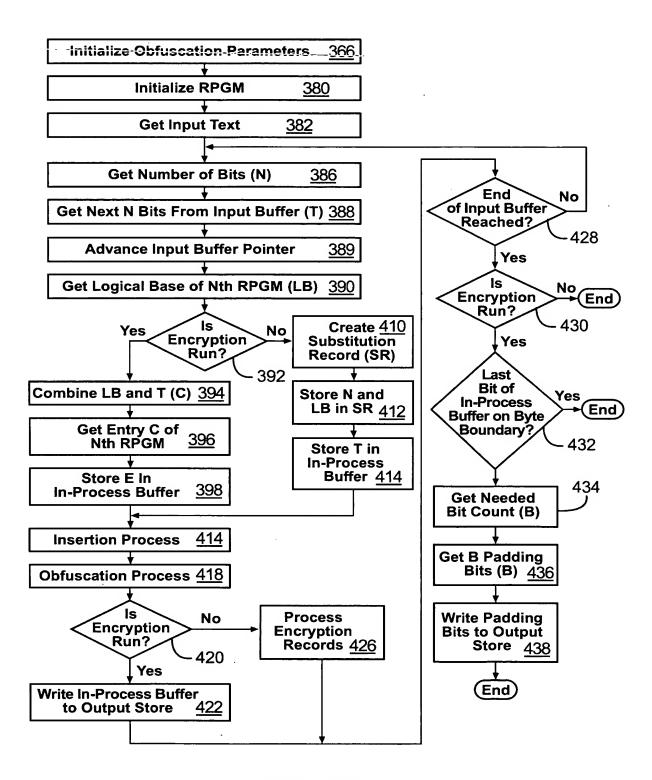
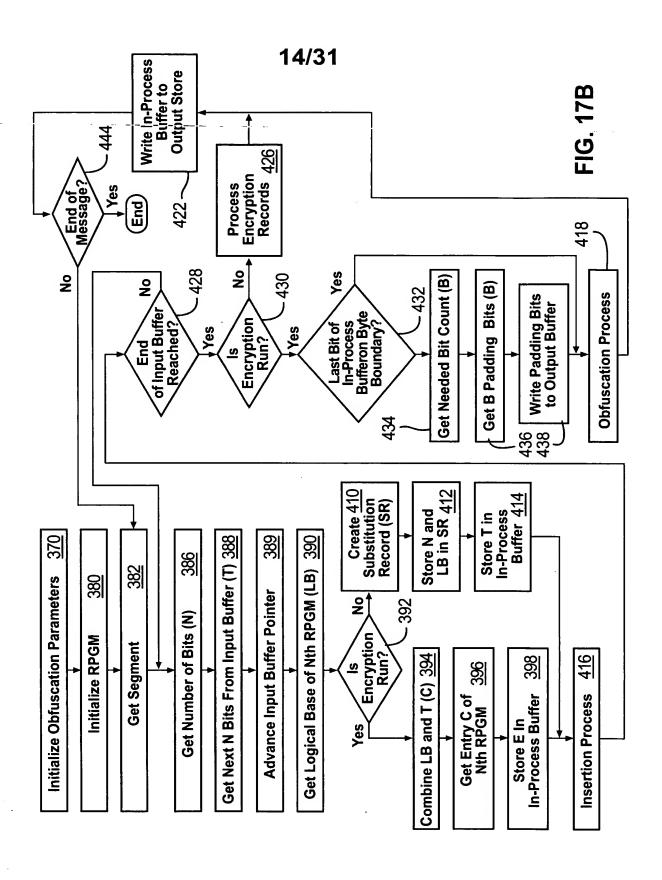


FIG. 16



**FIG. 17A** 



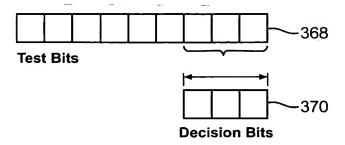


FIG. 18

### **Initialize Obfuscation Params**

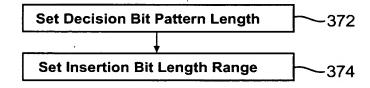
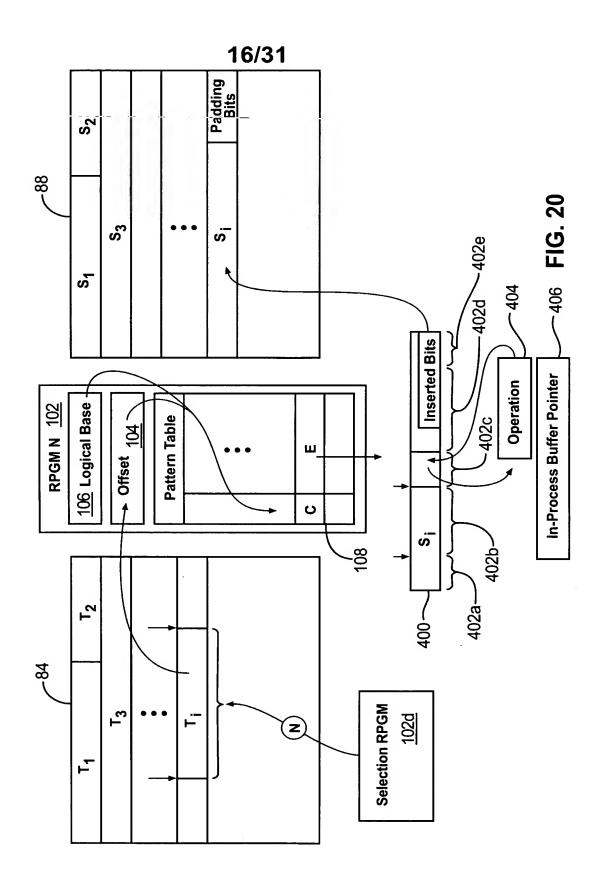


FIG. 19



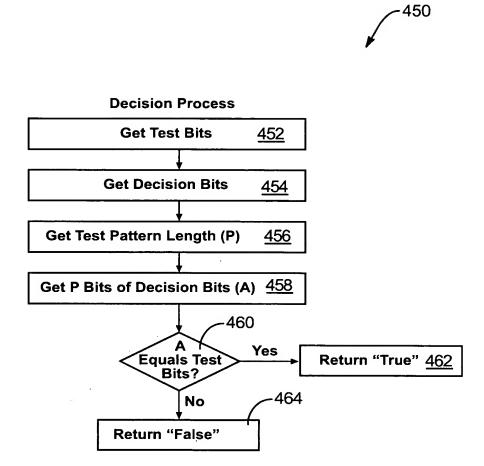


FIG. 21

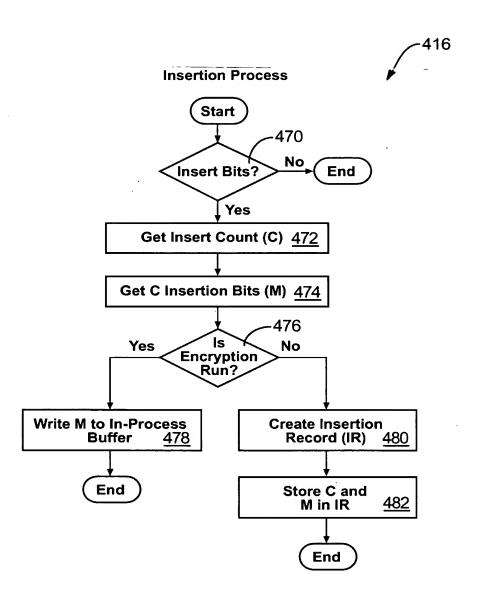


FIG. 22

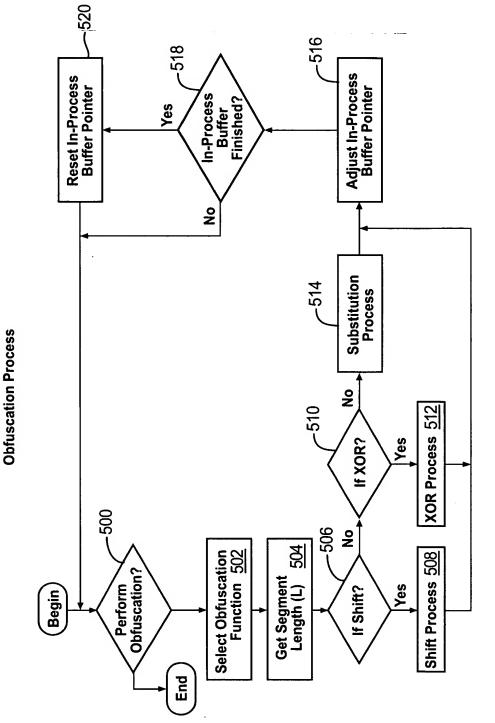


FIG. 23

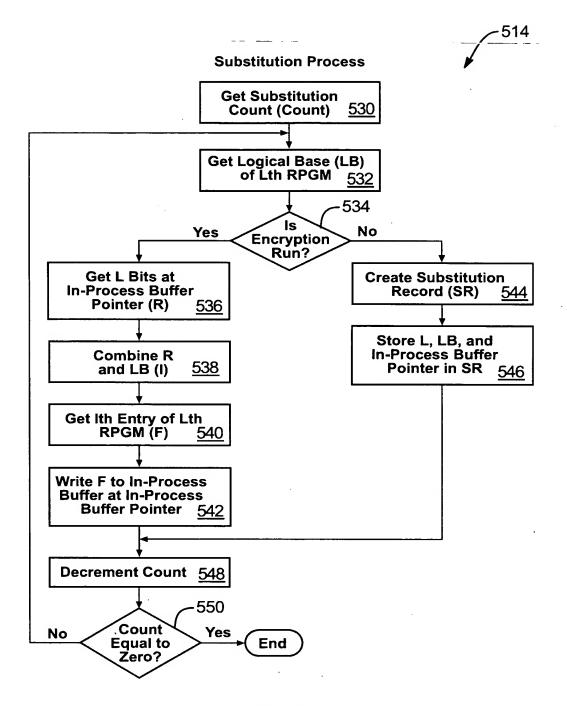


FIG. 24

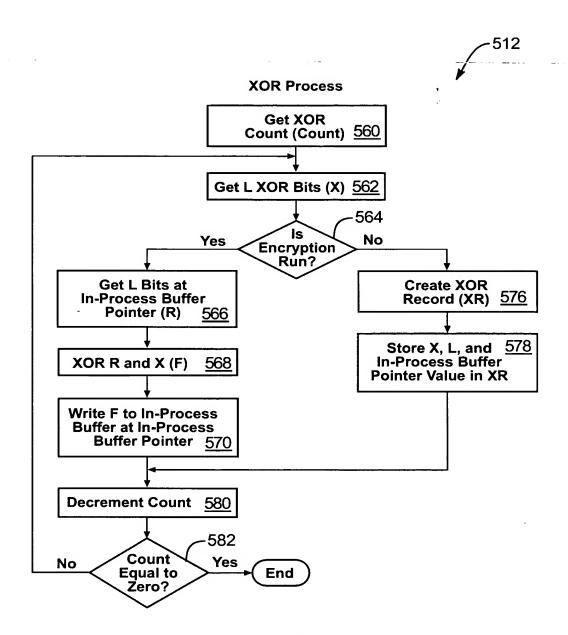
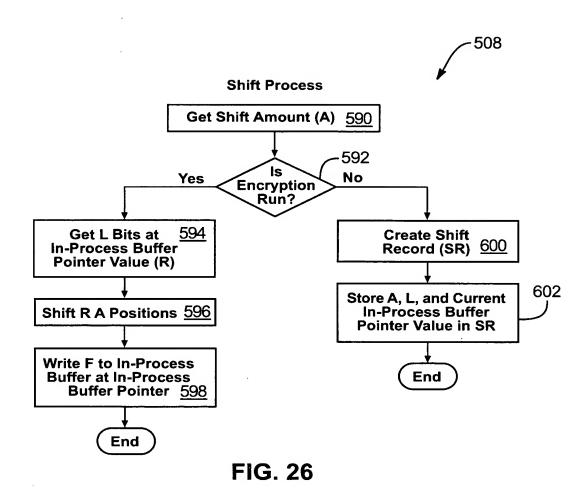


FIG. 25



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Encryption Record 610	!
- Substitute-Record— <u>612a</u>	]_
XOR Record 614a	
Shift Record 616a	]
Shift Record 616b	
XOR Record 614b	
Substitute Record 612b	
Shift Record 616c	]
Substitute Record 612c	]
Insertion Record 618	612d
Final Substitute Record	H

FIG. 27

Substitute Record	<u>612</u>
Number of Bits	<u>624</u>
Logical Base	<u>626</u>
Segment Address	<u>628</u>
Status (Final/Non Fina	i) <u>630</u>

Insertion Record	<u>618</u>
Number of Bits	<u>638</u>
Insertion Bits	<u>640</u>
Segment Address	<u>642</u>

FIG. 29

FIG. 28

Shift Record	<u>616</u>
Number of Bits	<u>650</u>
 Shift Amount	<u>652</u>
Segment Address	<u>654</u>

XOR Record	<u>614</u>
Number of Bits	<u>660</u>
XOR Bits	<u>662</u>
Segment Address	<u>664</u>

FIG. 30

FIG. 31

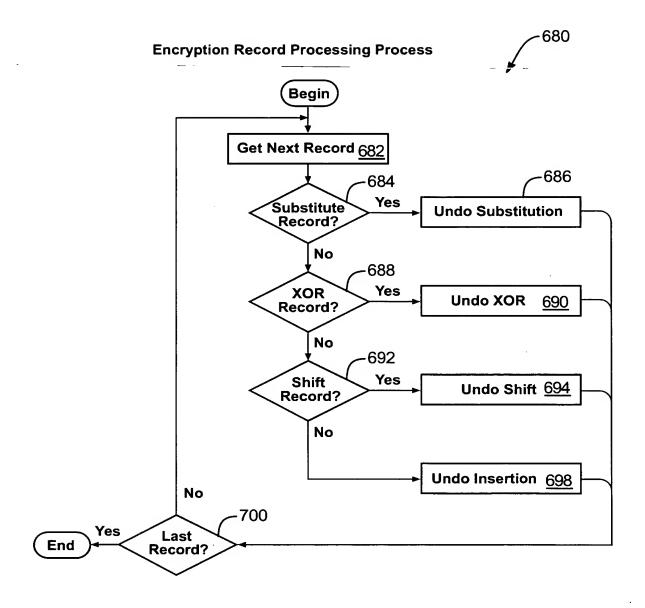


FIG. 32

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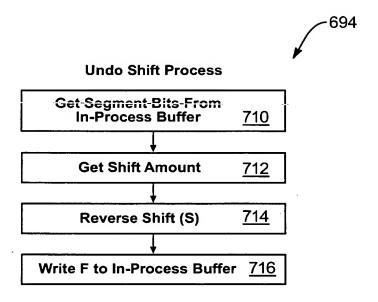


FIG. 33

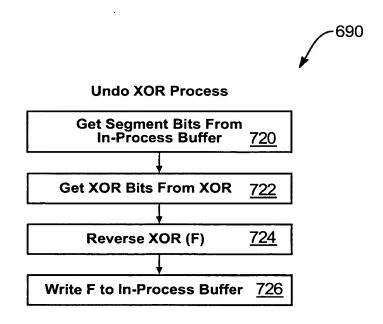


FIG. 34

### **Undo Insertion**

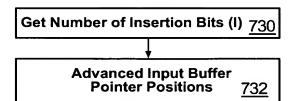


FIG. 35

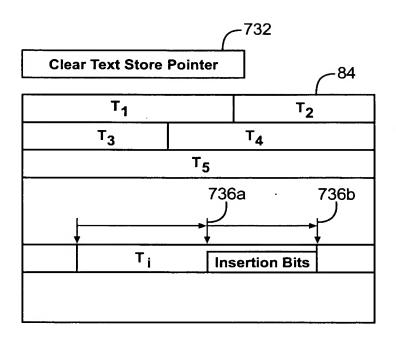


FIG. 36

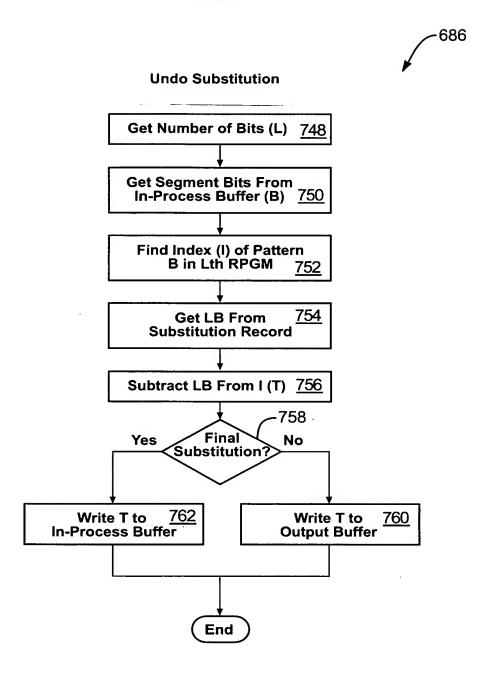


FIG. 37

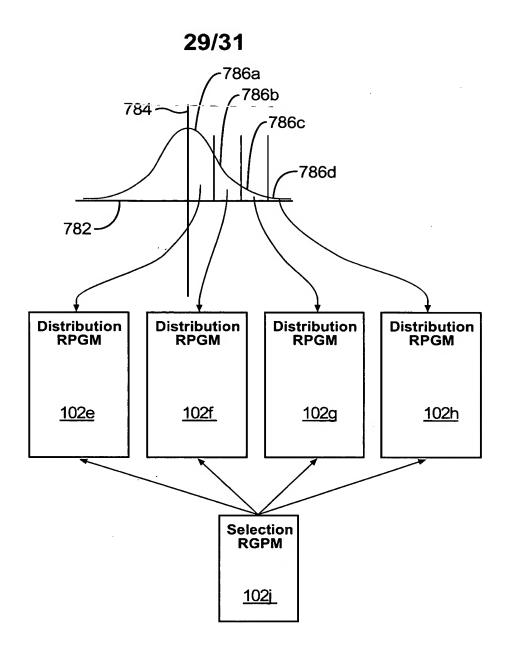
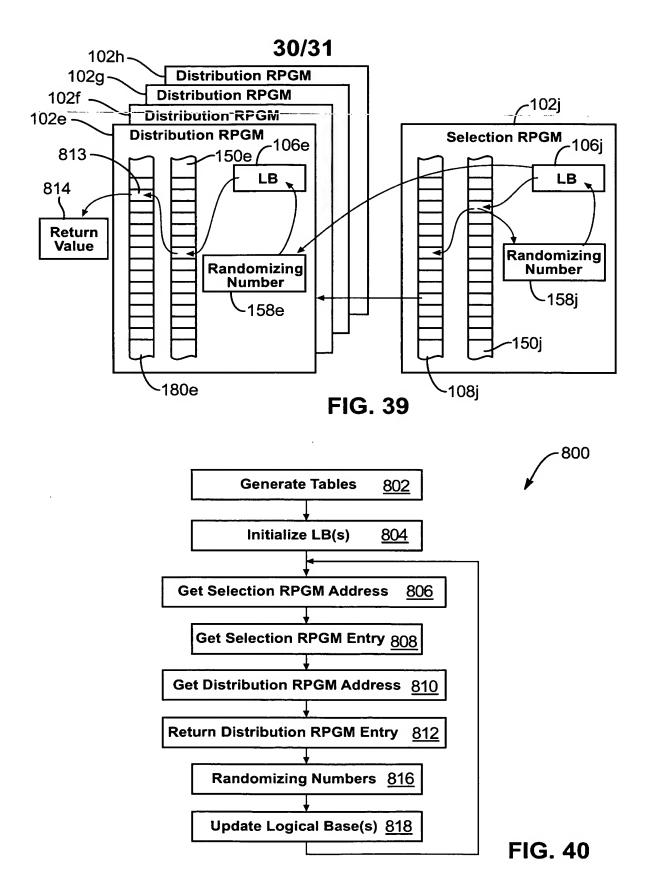


FIG. 38



826	828		830	
		Address Table		
Selecti RPGI		Randomining Number	Logical Base	
STD	1	Randomining Number	Logical Base	
•		•	•	

FIG. 41